#### REMARKS

## I. Allowable Subject Matter

The Applicant appreciates the Examiner's finding that claim 3 would be allowable if rewritten in independent form and including all of the limitations of the base claim and any intervening claim. Claim 3 has thus been amended to include the limitations of claims 1 and 2, and thus is presently in condition for allowance.

# II. Claim Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1-2 and 4-10 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent 5,491,474, issued to Neidlinger et al. ("Neidlinger") in view of K. Kaede et al., "A Passive Double Star Optical Subscriber System With Frequency Division Duplex Transmission And Flexible Access," IEICE Trans. Commination Vol. E75-B No. 9, Sept. 1992 ("Kaede"). The Examiner also rejected claim 11 under 35 U.S.C. § 103 as being unpatentable over Neidlinger in view of U.S. Patent 5,896,211, issued to Watanabe ("Wantanabe").

Claim 1, 2, 5, 8 and 9 have been cancelled. Claims 4 and 6 have been amended to depend from independent claim 3. Accordingly, claims 4 and 6 are thus presently in condition for allowance, as they depend from an allowable independent base claim.

Claim 7 has been amended to recite that the clock multiplier multiplies the clocking pulse by at least three times, and now includes the limitation "wherein said Manchester coded data stream includes three (3) pulses for each data bit and the Manchester decoding device is adapted to vote said three (3) pulses to determine at least two (2) equivalent pulses and provide an output NRZ data bit at said selected clocking pulse rate equivalent to said at least two (2) equivalent Manchester data bits."

The Applicant submits that the cited references, either alone or in combination, fail to disclose, teach or suggest these limitations. Accordingly, claim 7 is in condition for allowance. Claims 10 and 11, which depend either directly or indirectly form claim 7, are likewise in condition for allowance.

### III. New Claims 12-20

New claims 12-20 are presented for examination.

With respect to claim 12, the Applicant submits that the cited references, either alone or in combination, fail to disclose, teach or suggest "converting the second digital data from the second data code to the first data code by setting each bit of the second digital data in the first data code equal to a majority of corresponding bits of the second digital data in the second data code." Claim 12 is therefore allowable. Claims 13-15, which depend either directly or indirectly form claim 12, are likewise in condition for allowance.

With respect to claim 16, the Applicant submits that the cited references, either alone or in combination, fail to disclose, teach or suggest "means for converting the second digital data from the second data code to the first data code by setting each bit of the second digital data in the first data code equal to a majority of corresponding bits of the second digital data in the second data code." Claim 16 is therefore allowable.

With respect to claim 17, the Applicant submits that the cited references, either alone or in combination, fail to disclose, teach or suggest the step of "for each data bit of the second digital data in the first data code, including multiple corresponding data bits in the second digital data in the second data code and "converting the second digital data from the second data code to the first data code by setting each corresponding data bit of the second digital data in the first data code equal to a majority of equivalent bits in the multiple corresponding data bits in the

second data code." Claim 17 is therefore allowable. Claims 18 and 19, which depend either directly or indirectly form claim 17, are thus likewise in condition for allowance.

With respect to claim 20, the Applicant submits that the cited references, either alone or in combination, fail to disclose, teach or suggest "a first converting circuit configured to covert second digital data in the first data code to a second data code so that the power spectrum of the second digital data in the second data code is substantially separated from the power spectrum of the first digital data in the first data code and to include multiple corresponding data bits in the second digital data in the second data code" and "a receiver circuit configured to receive the second digital data in the second data code and convert the second digital data from the second data code to the first data code by setting each corresponding data bit of the second digital data in the first data code equal to a majority of equivalent bits in the multiple corresponding data bits in the second data code." Claim 20 is therefore allowable.

### IV. Conclusion

The Applicant respectfully submits that all pending claims are in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance in due course.

The Commissioner is hereby authorized to charge any additional fees and credit any overpayment associated with this response to Jones Day Deposit Account No. 501432, ref: 560043-610132.

Respectfully submitted,

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